ABSTRACT OF THE DISCLOSURE

A first concave portion for the element isolation, a second concave portion for an aligning mark, and a third concave portion for an anti-fuse portion are formed simultaneously within a silicon substrate. After a silicon oxide film is formed on the entire surface, the silicon oxide film positioned within the second and third concave portions is removed. Then, a gate insulating film is formed on the entire surface, followed by forming a polysilicon film on the gate insulating film. Further, these polysilicon film and gate insulating film are selectively removed to form a gate electrode above an element region, an aligning mark portion in the second concave portion, and a gate electrode for an anti-fuse portion on the bottom surface of the third concave portion.